# PMC-CPU/440

# PowerPC<sup>™</sup> PrPMC Module with Gigabit Ethernet, USB, CAN



#### PowerPC AMCC PPC440EPx

- 2x 1000BASE-T Gigabit Ethernet
- · USB 2.0 High Speed interface, host or device
- RS-232 access via PMC-I/O connector
- CAN contolled by esd Advanced CAN Core (esdACC)
- 533 MHz PowerPC CPU with FPU

#### Higher Layer CAN Protocols

- CANopen® according to CiA® standard CiA 301
- DeviceNet®
- ARINC825 protocol

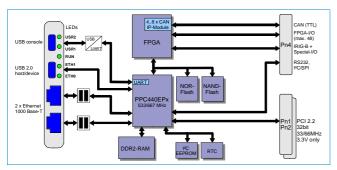
#### Various Interfaces and I/Os via Pn4

- 2...8x CAN interfaces
- RS-232 interface
- · IRIG-B time code interface

#### PMC PowerPC™ Board

The PMC-CPU/440 is a PCI Mezzanine Card that is automatically switched to monarch (PrPMC) or non-monarch mode according to the systems requirements. The PowerPC<sup>™</sup> AMCC PPC440EPx with 533 MHz or 667 MHz enables a performance of 1334 DMIPS peak. The board is equipped with at least 256 Mbyte DDR2 RAM and 256 Mbyte NAND Flash.

System time can be supported by RTC (with double layer capacitor) or IRIG-B. For CAN bus synchronisation tasks a high resolution CAN hardware timestamp is supported.





#### Connectivit

The PMC-CPU/440 comes with two Gigabit Ethernet interfaces that are accessible as 1000BASE-T via RJ45 connectors at the front panel. The PMC-CPU/440 provides 2...8 CAN interfaces controlled by an FPGA IP-Module. The CAN signals are available as TTL only via PMC connector. External converters from CAN-TTL to CAN-ISO11898 are available. All CAN interfaces allow data transfer rates up to 1 Mbit/s. An RS-232 serial port is available via the PMC-I/O connector. An USB 2.0 High Speed interface (host or device) is available at the front panel.

### Software Support

The flash memory carries the open source firmware 'U-Boot' that enables the PMC-CPU/440 to boot various operating systems from network or on-board Flash. Thus Linux®, VxWorks® (5.5 and 6.3), OS/9® and QNX® are directly supported with full support of onboard drivers by esd, others on request. There is also a bunch of higher layer protocols available like CANopen, DeviceNet. and ARINC825.

#### **Technical Specifications:**

PMC interface a	and microprocessor:			
Microprocessor	AMCC PPC440EPx, 533/667 MHz, 32 bit			
Memory	256 Mbyte DDR2 RAM, 256 Mbyte NAND flash, 4 Mbyte NOR flash			
RTC	EPSON RX8025, backup by double layer capacitor			
PCI	PCI 2.2, 32 bit 33/66 MHz, signal voltage 3.3 V only, PrPMC acc. to Vita 32, monarch/non-monarch			
Connectors:				
Ethernet	2x 1000BASE-T, IEEE802.3, RJ45-connector			
USB	USB 2.0 High Speed interface, host or device			
Serial	1x serial console via local USB/serial converter, 1x RS-232 at PMC-I/O connector Pn4 (4-pin)			
CAN	28x CAN, controller FPGA IP module, ISO11898-1 (CAN 2.0), TTL-level signals, 1 Mbit/s, high resolution CAN-hardware timestamp (FPGA), PMC-connector			
IRIG-B	digital differential physical layer, IRIG B100 time code format, decoding and time code generation			

General:				
Ambient temp.	0 °C50 °C			
Humidity	max. 90 %, non-condensing			
Power supply	5 V, 3.3 V			
Connectors	PMC-connector Pn4: CAN, serial, IRIG-B, I <sup>2</sup> C front panel: 2x Mini-USB (console, host/device), 2x 1000BASE-T			

Order Informati	on:		
Hardware	Order No.		
PMC-CPU/440 PMC-CPU/440		h 2xCAN 533 ext.IO h 2xCAN 533	V.2027.02 V.2027.05
PIM-CPU/405	PIM I/O with 2x (	V.2025.02	
Software Suppo	rt 1		
PMC-CPU/440-VxW PMC-CPU/440-Linux PMC-CPU/440-QNX		VxWorks BSP Linux BSP QNX BSP	V.2027.30 V.2027.32 V.2027.33
ARINC object I ARINC825-L		cluding CD-ROM¹: rks	C.1140.18

1 For detailed information about the driver availability for your operating system please contact our sales team.

©2012 esd electronic system design gmbh Hannover
All data are subject to change without prior notice.
IATextelDokulDBLIPMC\Englisch\BLUE\PMC\CPU440\_Datasheet\_en\_12.wpd

 ${\sf CANopen^8}$  and  ${\sf CIA^8}$  are registered Community Trademarks of CAN in Automation e.V. All other trademarks are reserved by their respective owners.

esd electronic system design gmbh Vahrenwalder Str. 207 30165 Hannover / Germany Phone: +49 (0) 511 3 72 98-0 Fax: +49 (0) 511 3 72 98-68 E-mail: info@esd.eu

### PMC-CPU/440

## Driven by esdACC (Advanced CAN Core)

#### Basic Product Features:

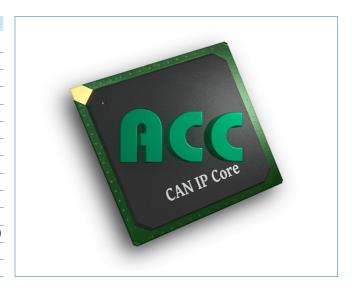
- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- · Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)

#### Superior esdACC Features:

- · Operating system independently programmable via esd's NTCAN-API
- · 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- · Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-Bit microcontroller to further relieve
- · Optional different sources for timestamps (e.g. IRIG-B)
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering'

(event on one CAN bus triggers event on another bus)

- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.



#### Driver Availability:

Windows, Linux<sup>1</sup>, QNX<sup>1</sup>, VxWorks<sup>1</sup>, RTX<sup>1</sup>

For detailed information about the driver availability for your operating system and the particular esd CAN interface please contact our sales team

#### Available higher level protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

30165 Hannover / Germany

Vahrenwalder Str. 207

E-mail: info@esd.eu